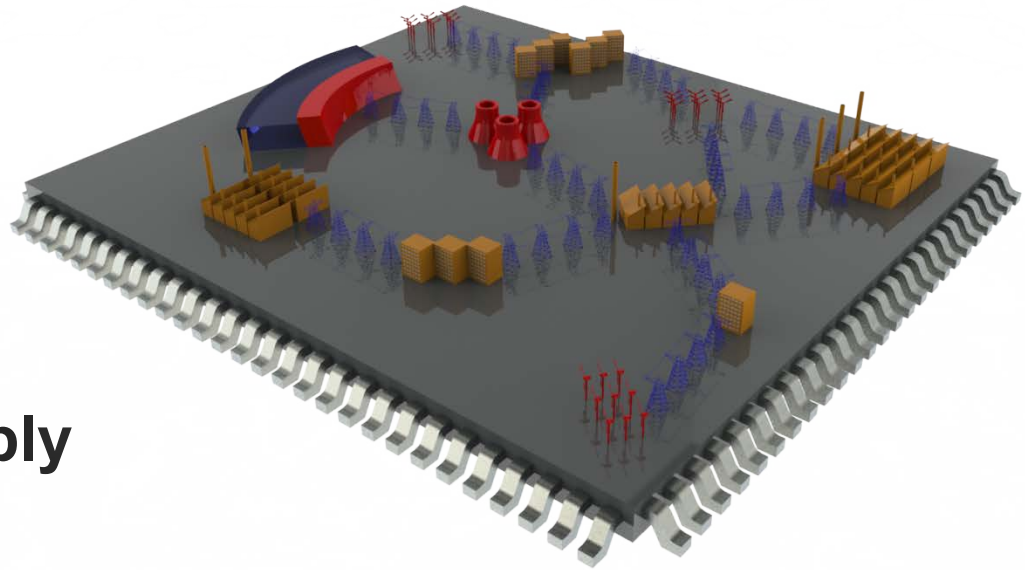
High-speed, mixed signal emulation for power system dynamic analysis

Prof. M. Kayal

Dr R. Cherkaoui



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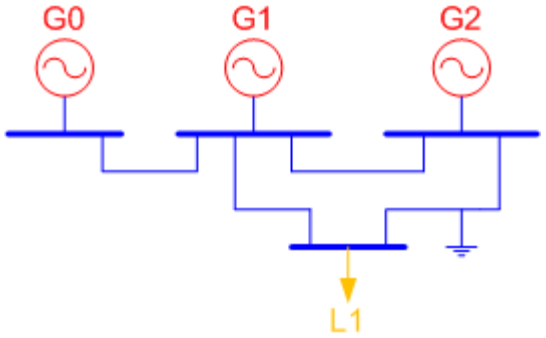
Outline

1. Electronics Emulation of power system
2. Field Programmable Power Network System (FPPNS) approach
3. Mixed signal phasor implementation:
   - Hardware and software
4. Fully analog implementation
5. Demonstration
6. Conclusion

Project objectives

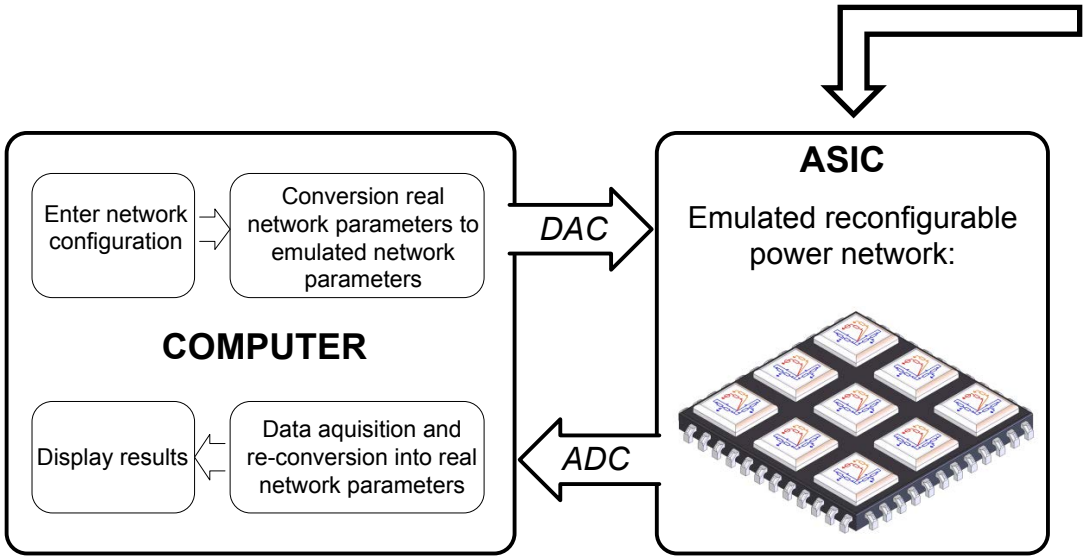
- Analysis of the potential applications of adding dedicated computation electronics for **real-time power systems**.
- Using the dynamic stability computation as a case study:
  - Very demanding in simulation time.
  - Simulation time is proportional to the number of nodes.
- Creating a modular and flexible hardware approach.
- Programmability is a target

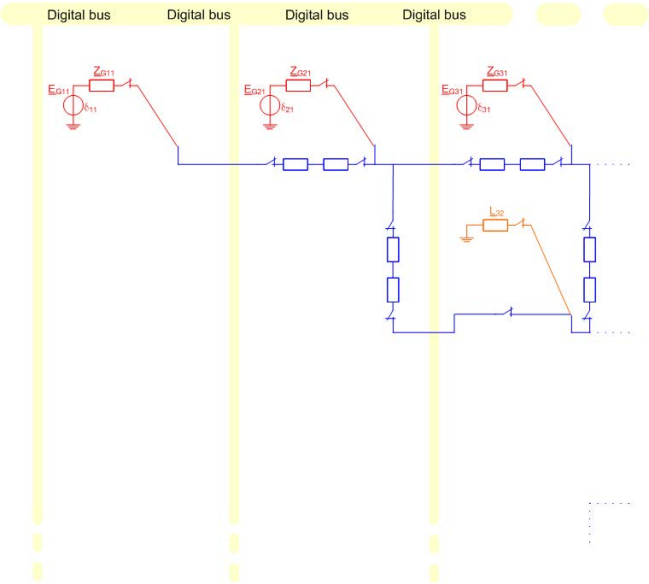
Project objectives



- **Power network theory**
  Generators, loads and transmission lines

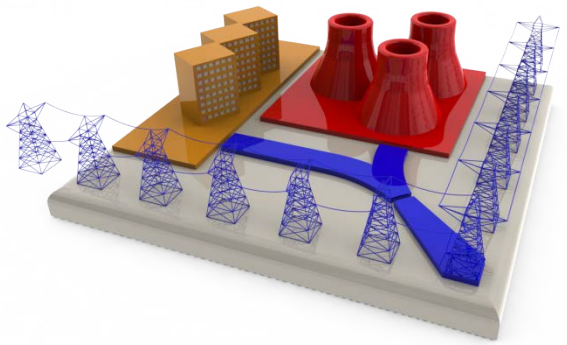
- **Programmable and modular emulator (patented with ABB)**
  FPPNS (Field programmable power network system)



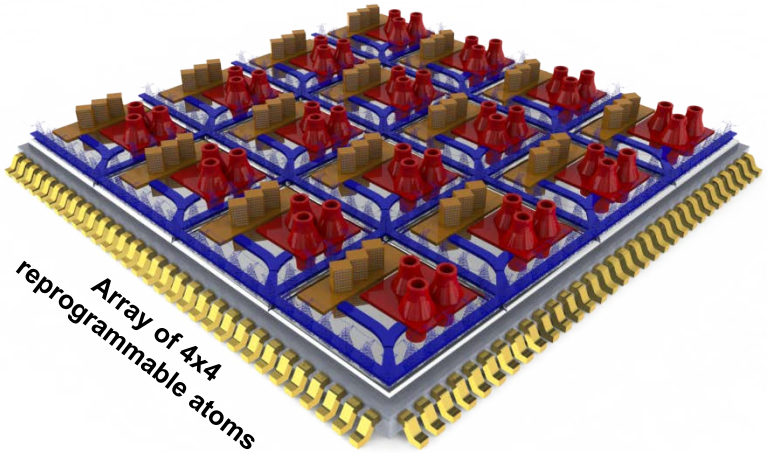


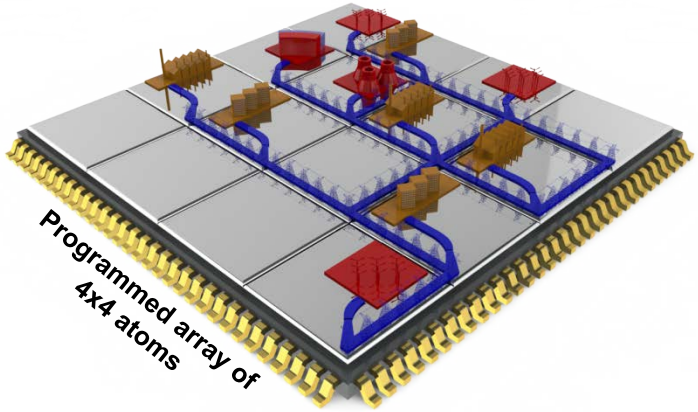
Reprogrammable atom – the concept

- **Modular system**
  Based on reprogrammable atoms
  Programmable components
  Generator + Load + Lines



- **Programmable and modular emulator**
  FPPNS (Field programmable power network system)

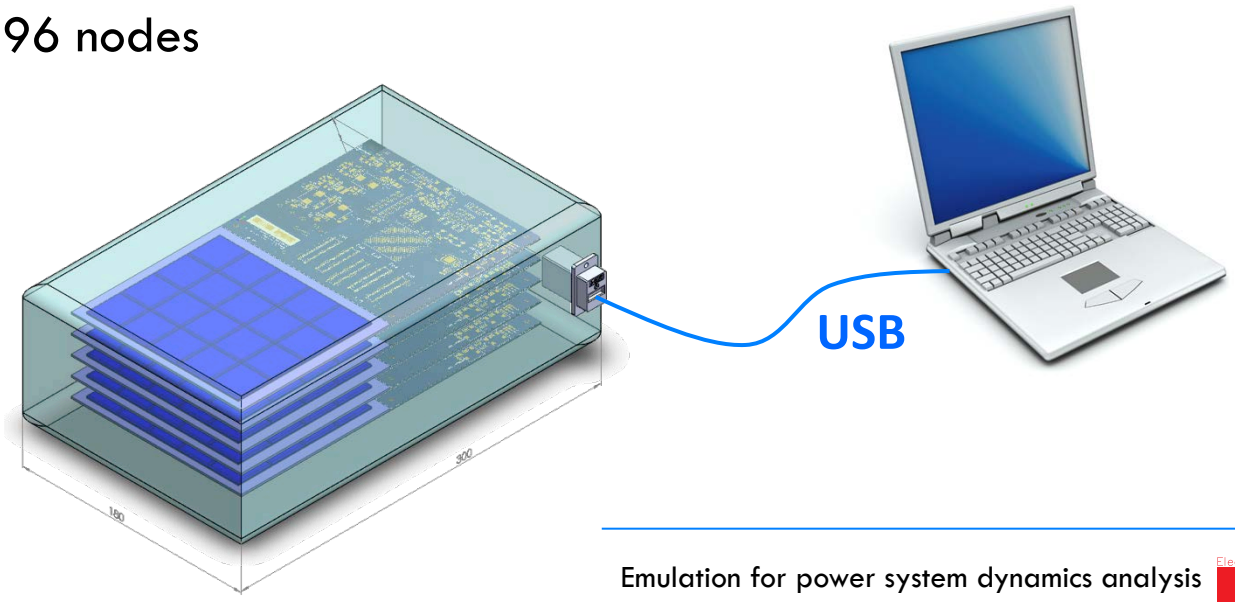




Hardware and software development

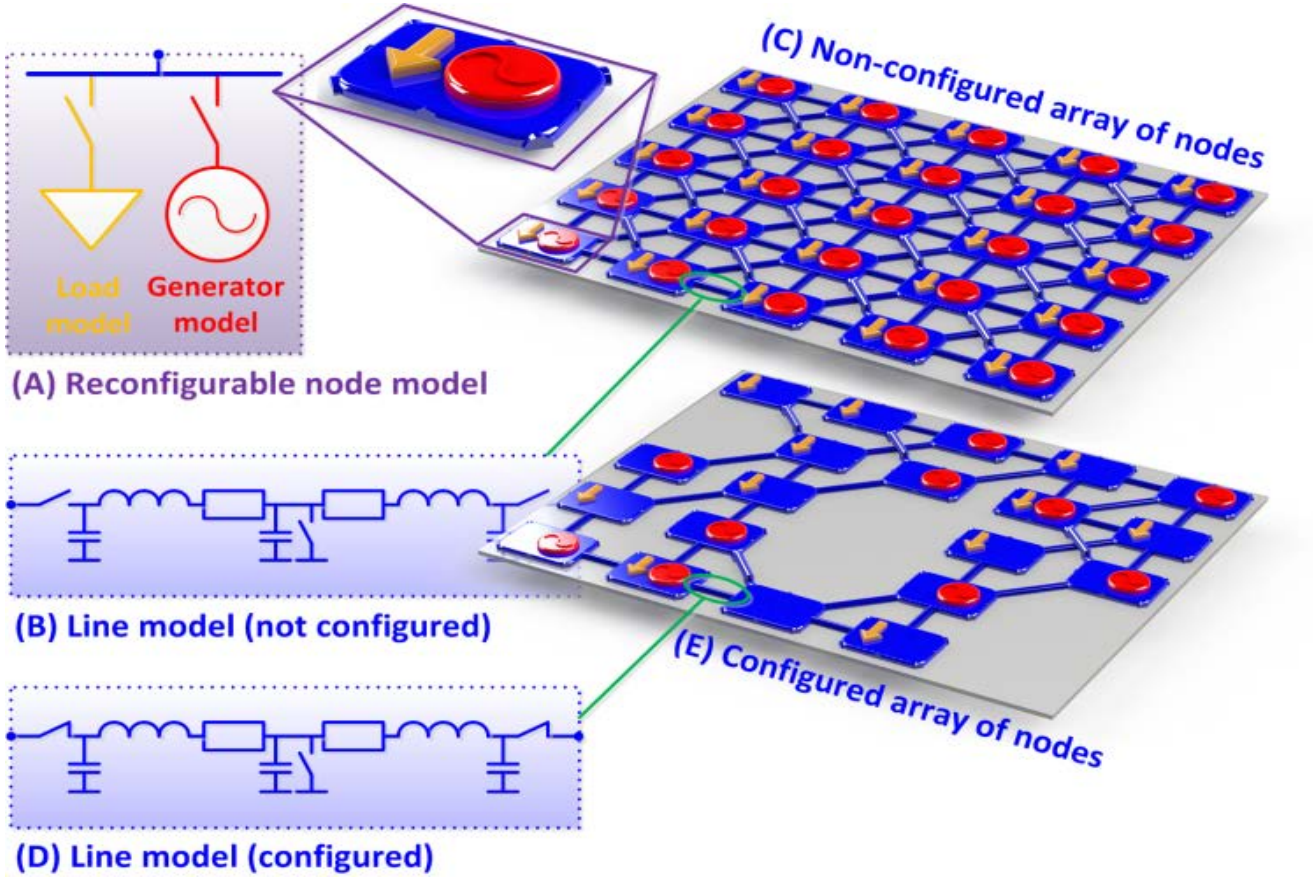
- Based on 4x24 nodes mixed-signal emulation platform
  - Analog computation of the grid
  - Digital computation for the model of power system nodes
  - ADCs and DACs links analog and digital

- Prototype targets dynamics power system computation
  - Up to 1000x faster than real-time
  - Up to 96 nodes



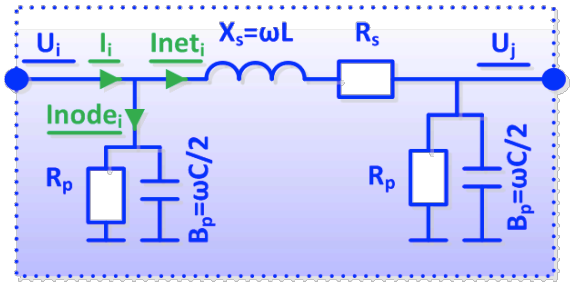
A reconfigurable array of nodes

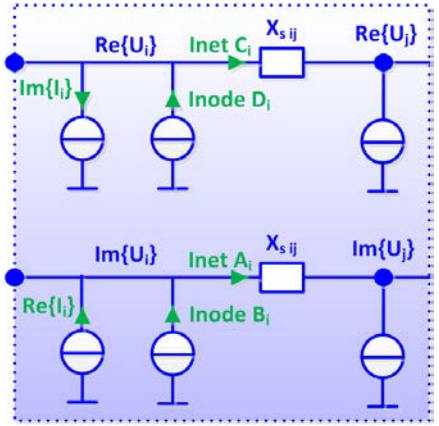
- FPPNS (Field programmable power network system)
- Network topology configured through analog switches



Hybrid (mixed-signal) phasor emulation

➢ Analog modeling of the RLC Π -line

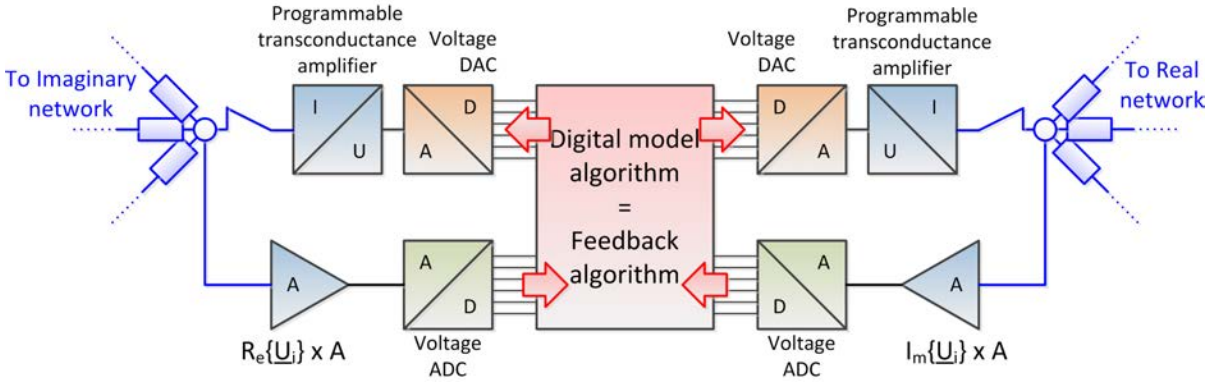




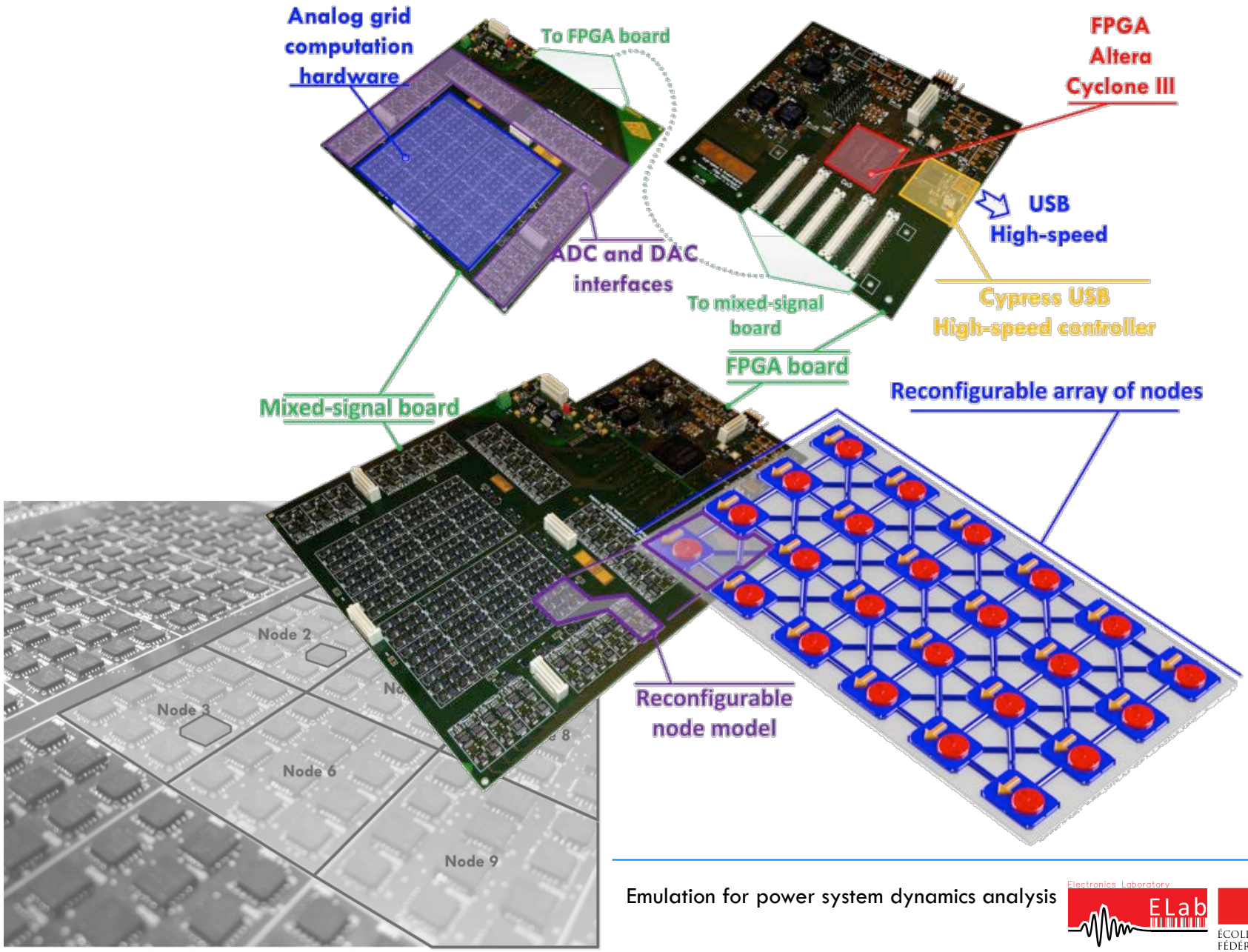
$$\Re e\{\underline{I}_i\} = \underbrace{\sum_{j=1}^{n}\left(\frac{X_{S_{ij}}}{R_{S_{ij}}^2 + X_{S_{ij}}^2}\cdot\left(\Im m\{\underline{U}_i\} - \Im m\{\underline{U}_j\}\right)\right)}_{I_{net\ A}} - \underbrace{\left(B_{P_i}\cdot\Im m\{\underline{U}_i\}\right)}_{I_{node\ B}}$$

$$j\cdot\Im m\{\underline{I}_i\} = -j\cdot\underbrace{\sum_{j=1}^{n}\left(\frac{X_{S_{ij}}}{R_{S_{ij}}^2 + X_{S_{ij}}^2}\cdot\left(\Re e\{\underline{U}_i\} - \Re e\{\underline{U}_j\}\right)\right)}_{I_{net\ C}} + j\cdot\underbrace{\left(B_{P_i}\cdot\Re e\{\underline{U}_i\}\right)}_{Network\ C}$$

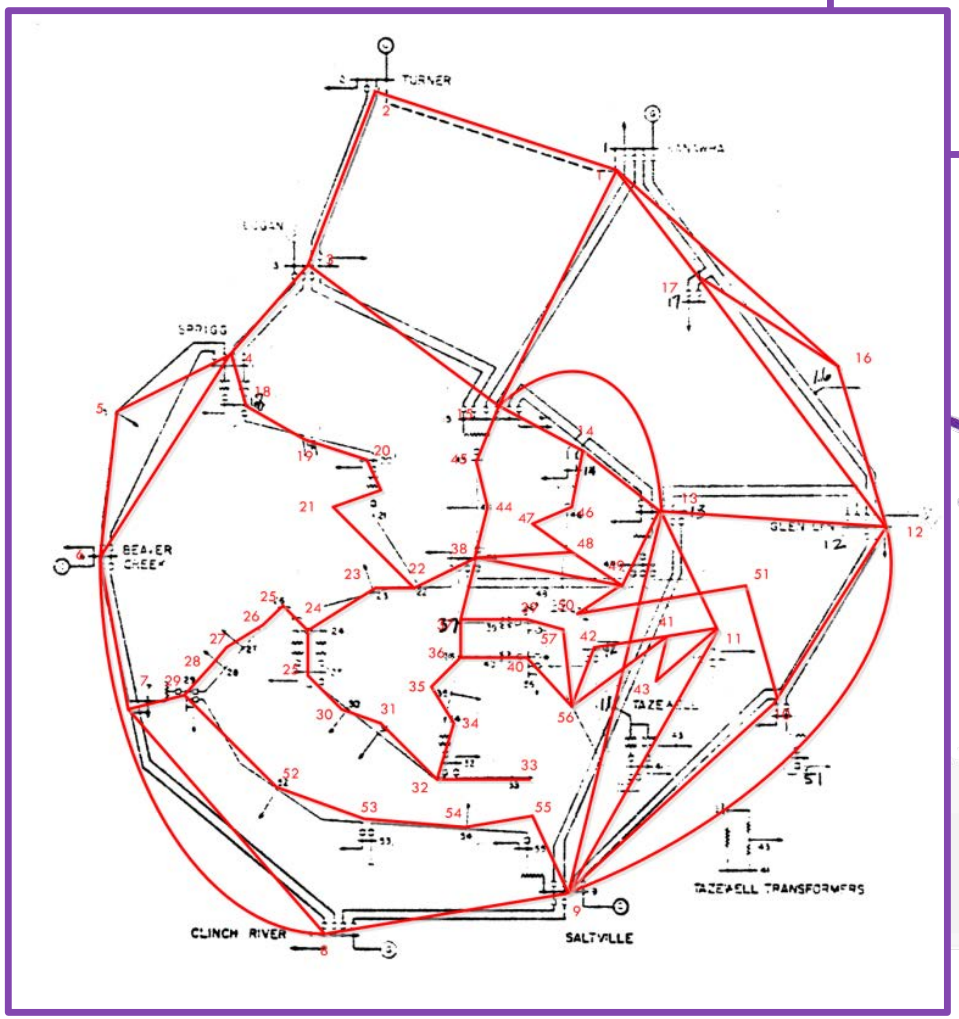
➢ Node interface



Hardware details – 24 nodes platform



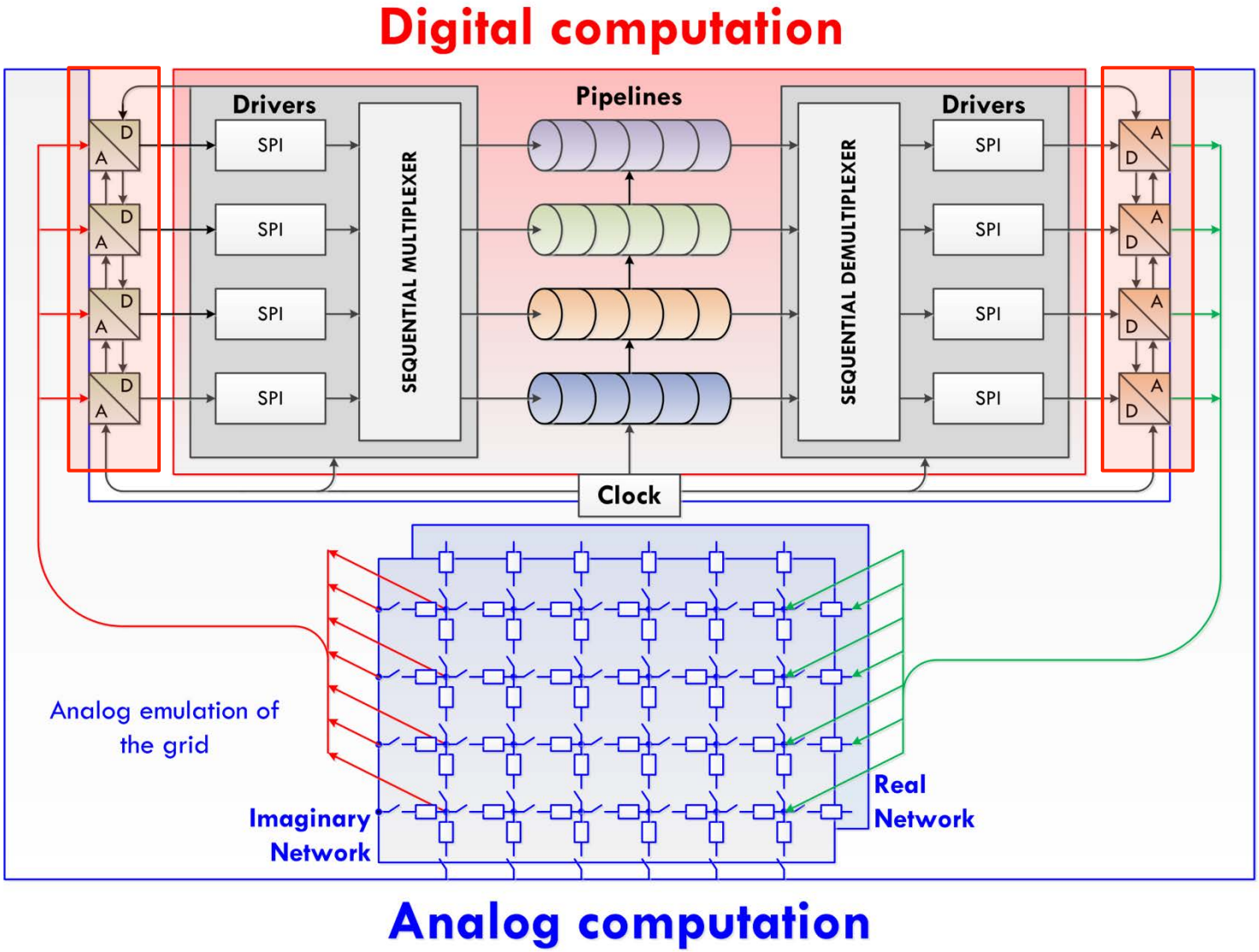
Hardware details – 4x24 nodes platform



57 IEEE reference topology

96 nodes mixed-signal hardware platform

FPGA parallel pipelined



State-of-the-art

- Multicores architectures
- GPU architectures
- CPU + GPU architectures
- **Mixed-signal emulation**

Speed limitation: Access time to memory

Speed limitation: ADCs and DACs speed

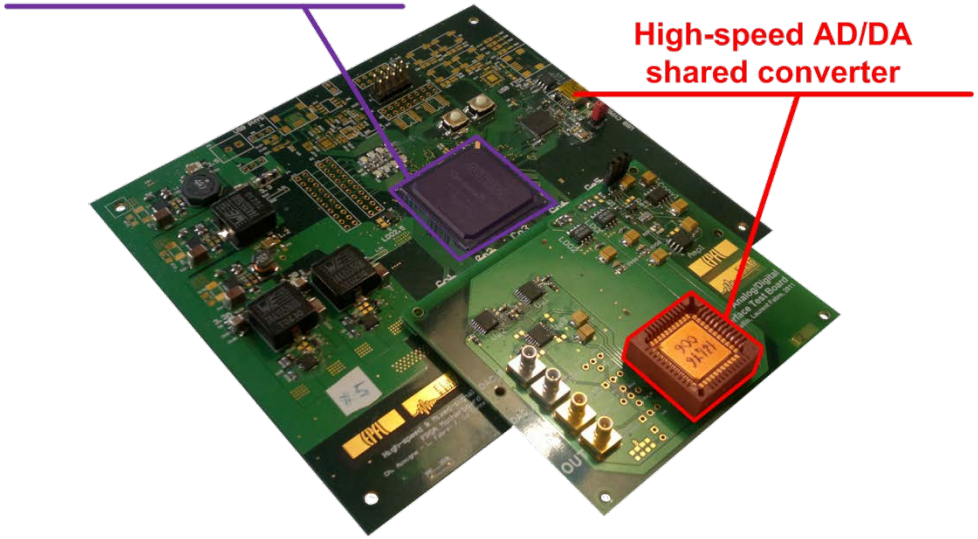
System size versus computation time. Simulation duration of 1580 ms. Speed defined as "faster than real-time"

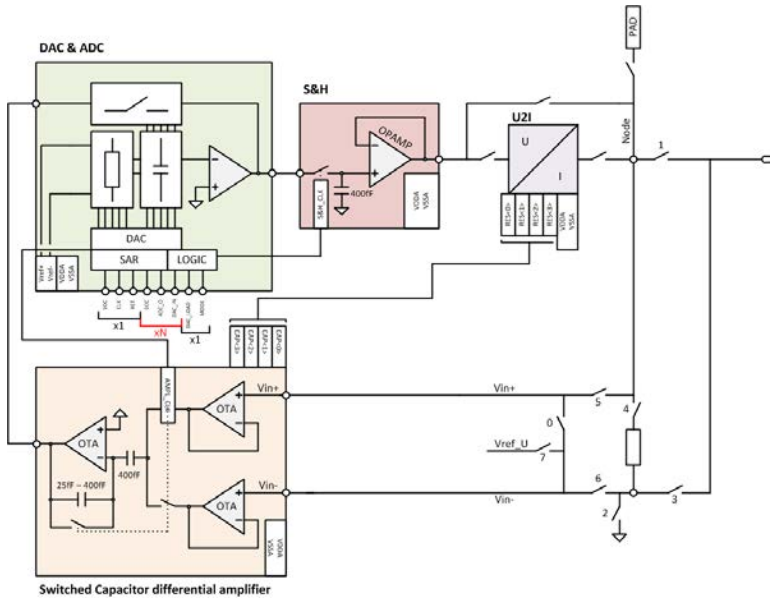
System scale	Generators	Buses	Multicores PSS/E	CPU C++	GPU CUDA	GPU & CPU CUDA based
1	10	39	4.50 x	1.76 x	0.28 x	0.56 x
2	20	78	3.95 x	0.24 x	0.2 x	0.3 x

EPFL/ABB x1000

Test board for high-speed AD/DA shared converters

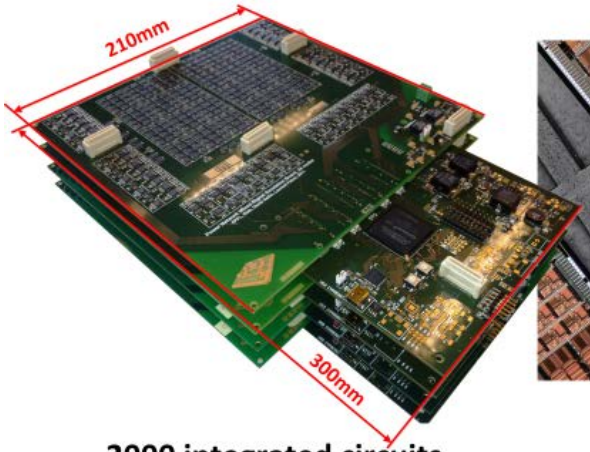
- Further increase speed of AD and DA converters
- Reducing converter area
- FPGA drivers can be reuse





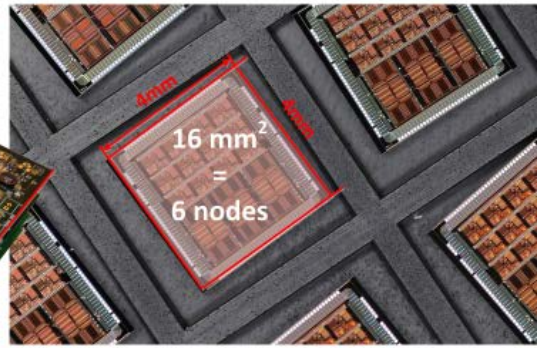
24 nodes integrated platform

- Contains 4x6 integrated nodes
- Can be directly plugged on the FPGA board
- Increase of signal-on-noise ratio
- Reduces costs and complexity

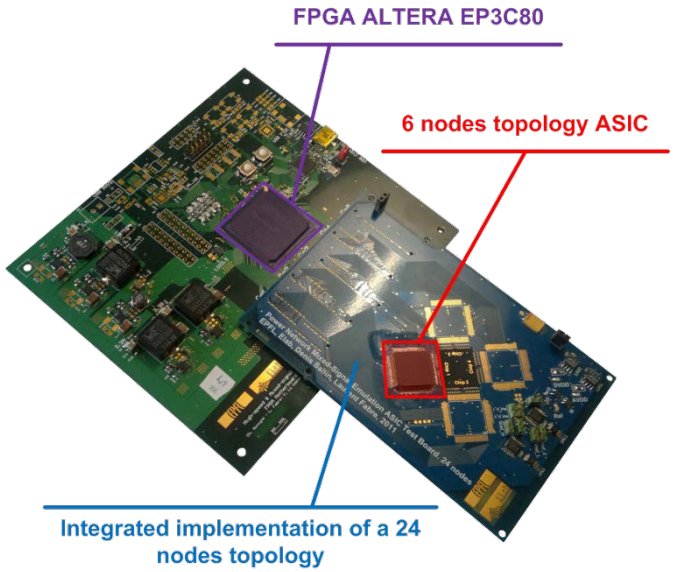


2000 integrated circuits
252'000 mm^2 for 96 nodes

~ 20 KFr / 96 nodes

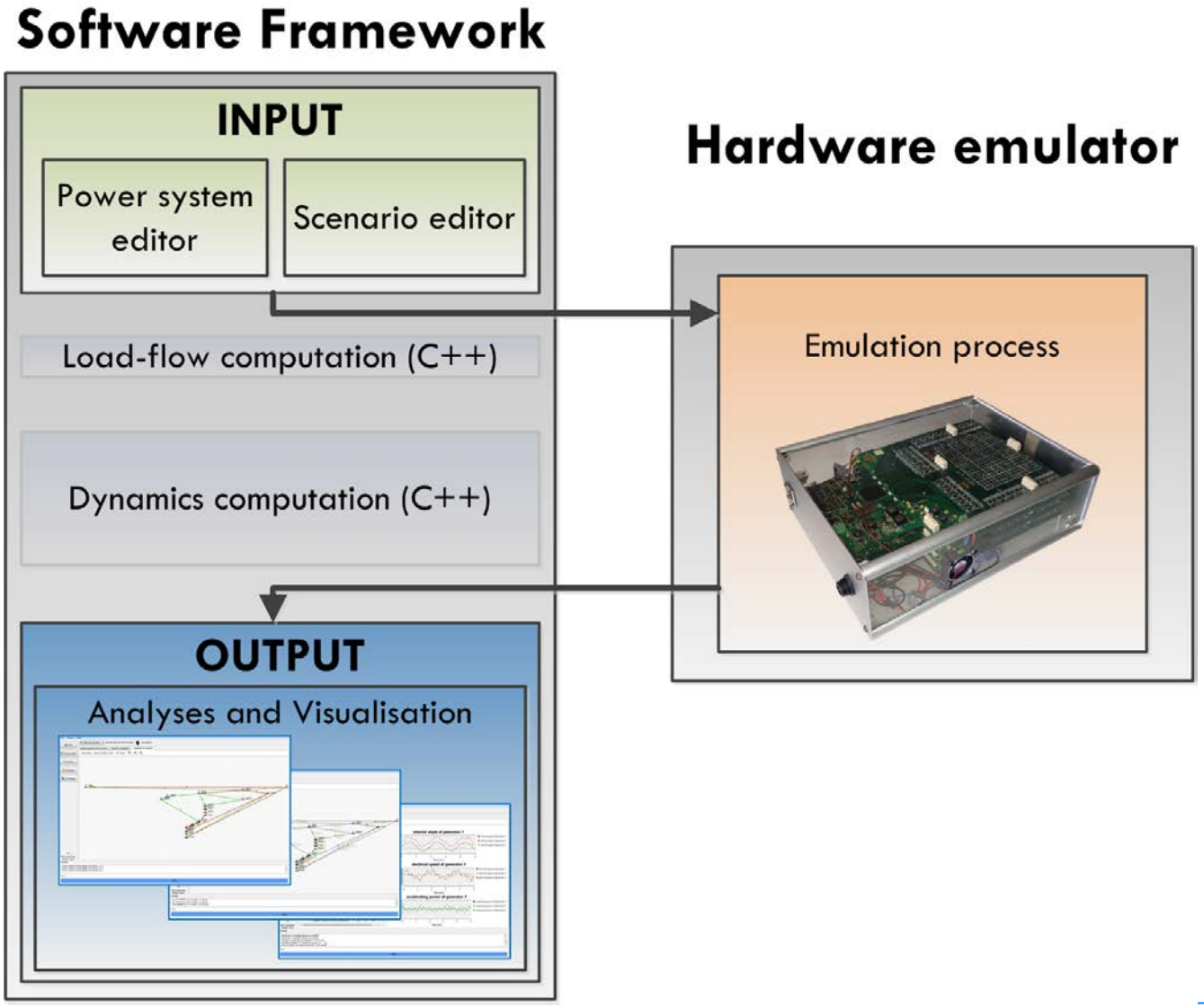


16 integrated circuits
256 mm^2 for 96 nodes

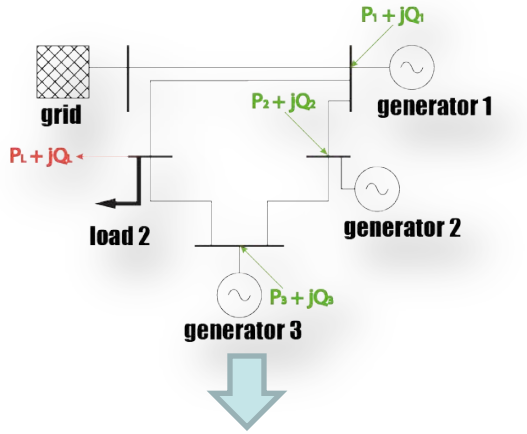


~ 5 KFr / 96 nodes

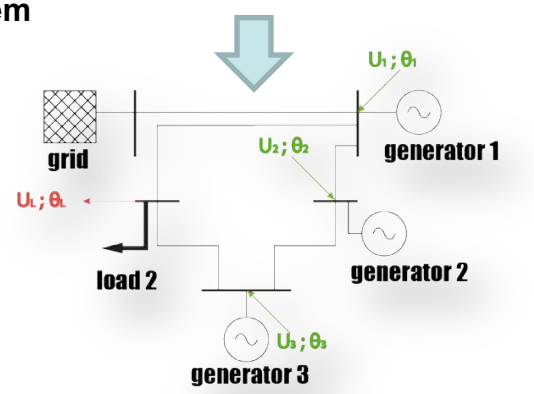
Software and graphical user interface

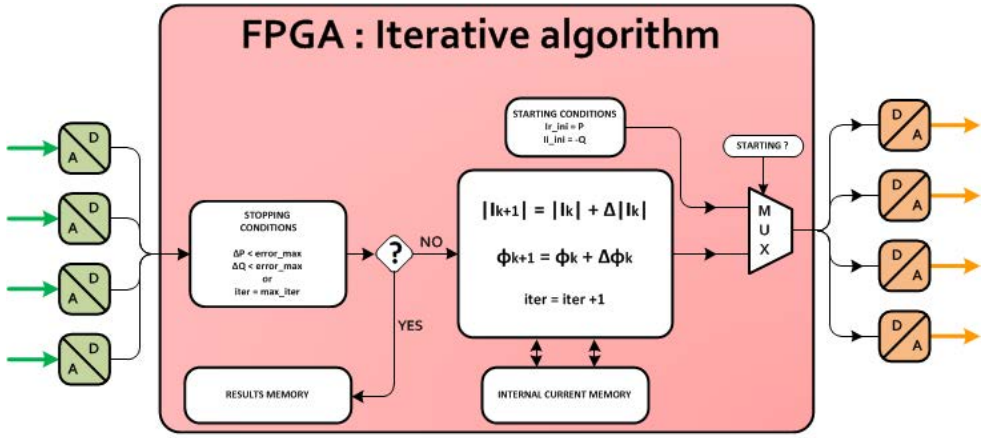


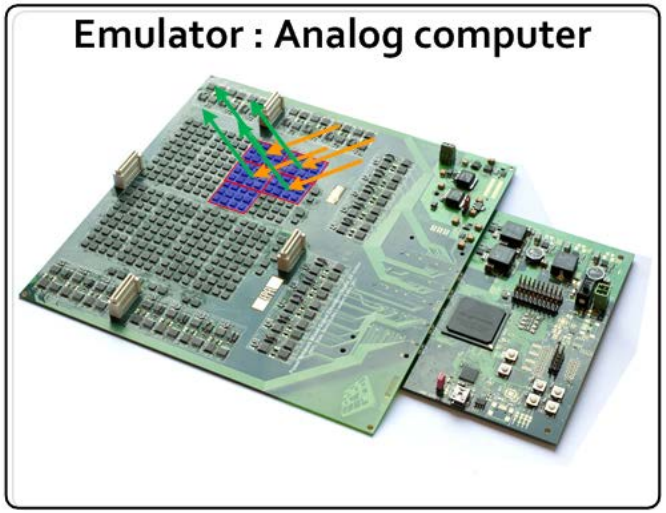
Load Flow Analysis



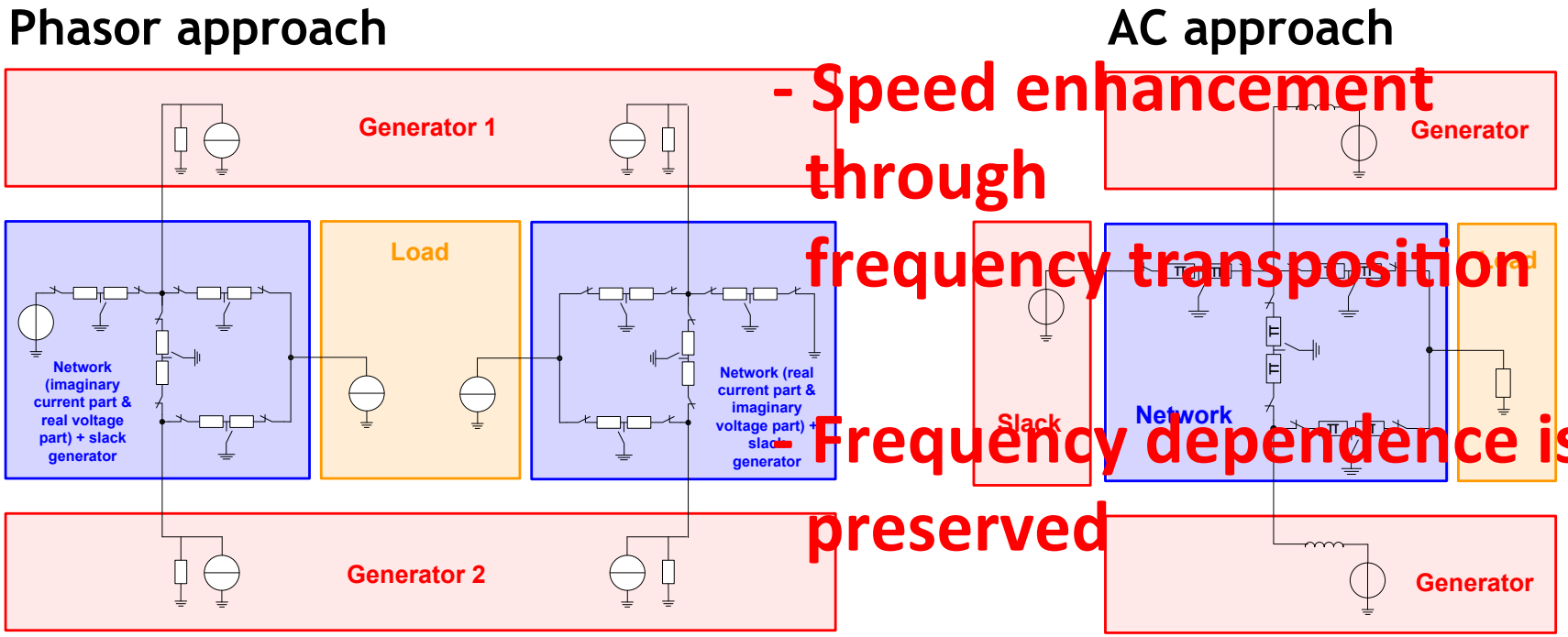
Power Injections (*P*-active and *Q*-reactive) the emulator coupled with an iterative algorithm permits to converge to the steady state of the system







AC emulation approach - Basics



- Speed enhancement through frequency transposition

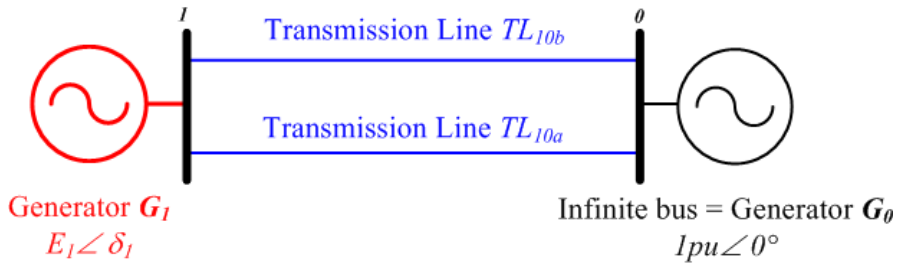
- Frequency dependence is preserved

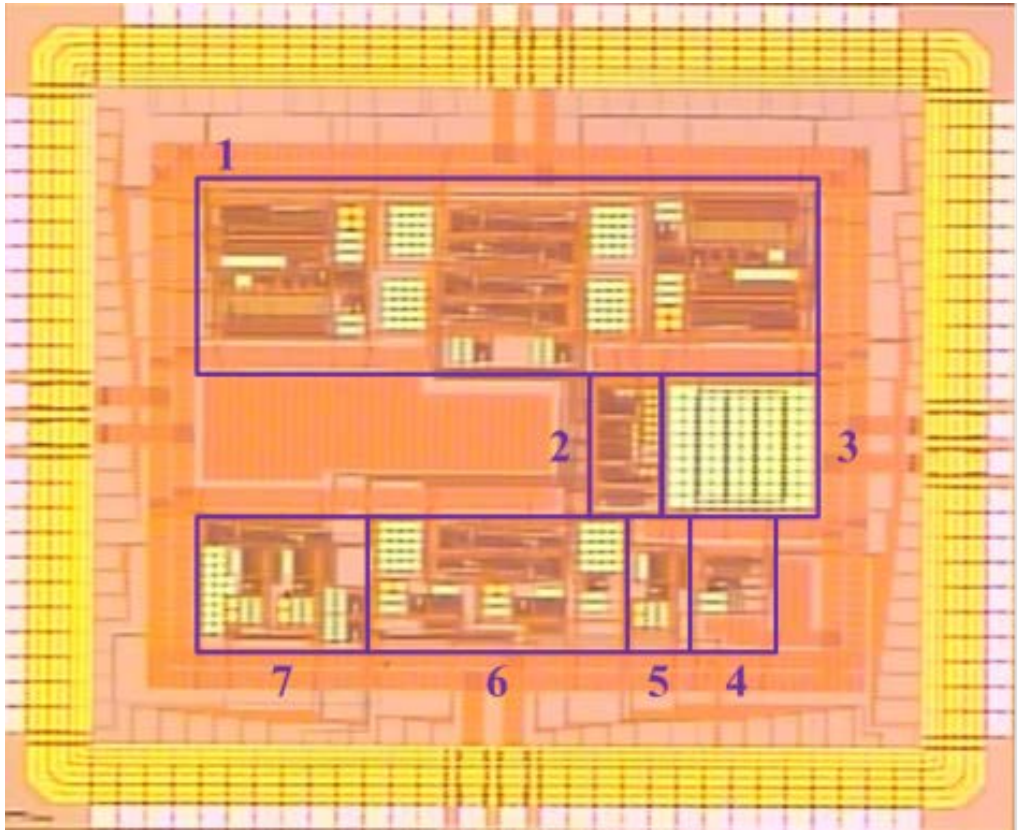
- First demonstrator limited to transient stability

Microelectronic implementation (purely analog or mixed mode) of power system's mathematical model.

Consisting of the real power system on chip by one-to-one mapping onto active microelectronics.

AC emulation approach – First demonstrator





CMOS AMS 0.35µm		
Supply Voltage	3.3	V
$Area_{block1}$	1.35	mm^2
$Area_{inductor}$	0.15	mm^2
$Area_{VCO}$	0.35	mm^2

Power Consumption (entire ASIC, 3.3V)		
unprogrammed	6.6	mA
Block I alone (steady state, max)	10.2	mA

Conclusions

- Dedicated electronics is definitely the way for real time solution.
- Integrated circuits is improving SNR for large scale power systems and Mixed mode (analog/digital) with:
  - Power system components modeled on digital
  - Connection in done on analog

- Next steps:
  - Targeting more nodes
  - Extending the emulation to other power system issue:
    - Optimization
    - Screening
    - Fault localization,….