RIE Plenary Assembly
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General aspects of the real-time simulation of electrical systems

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Hardware-in-the-Loop

Numerical solvers

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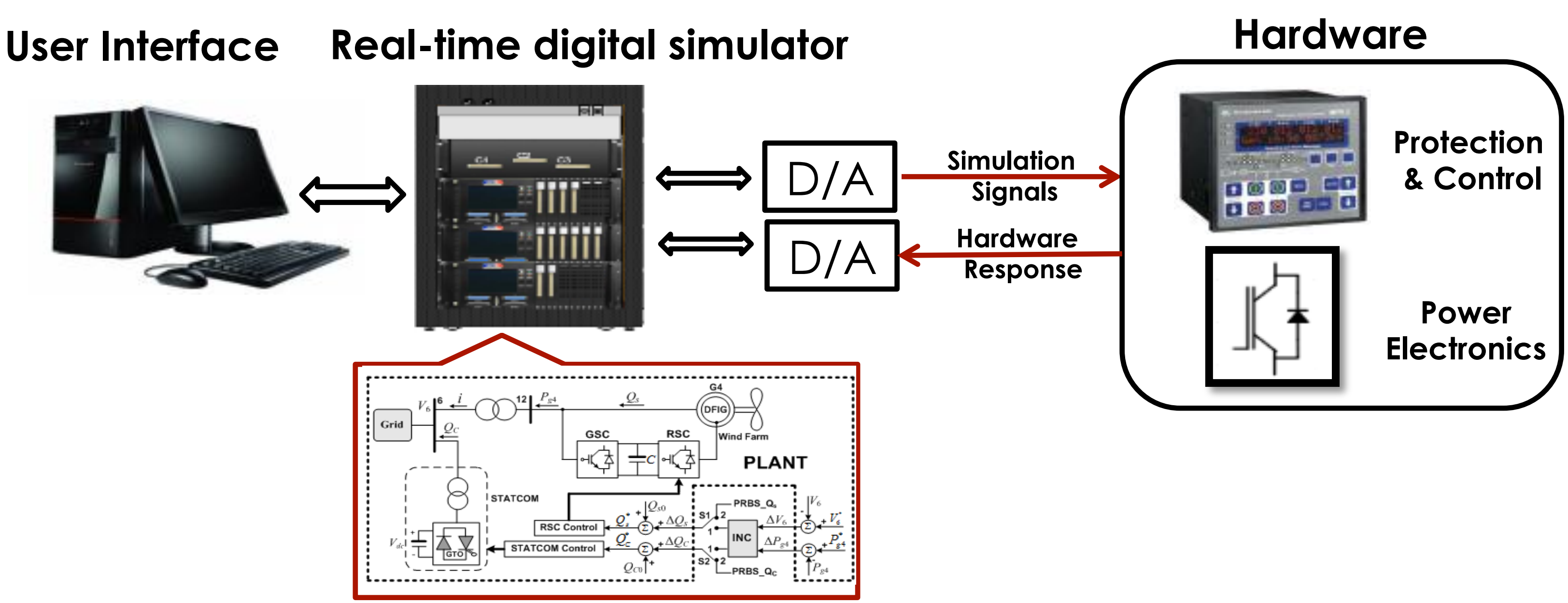
Hardware-in-the-Loop (HIL)

What is the concept of “HIL simulation”?

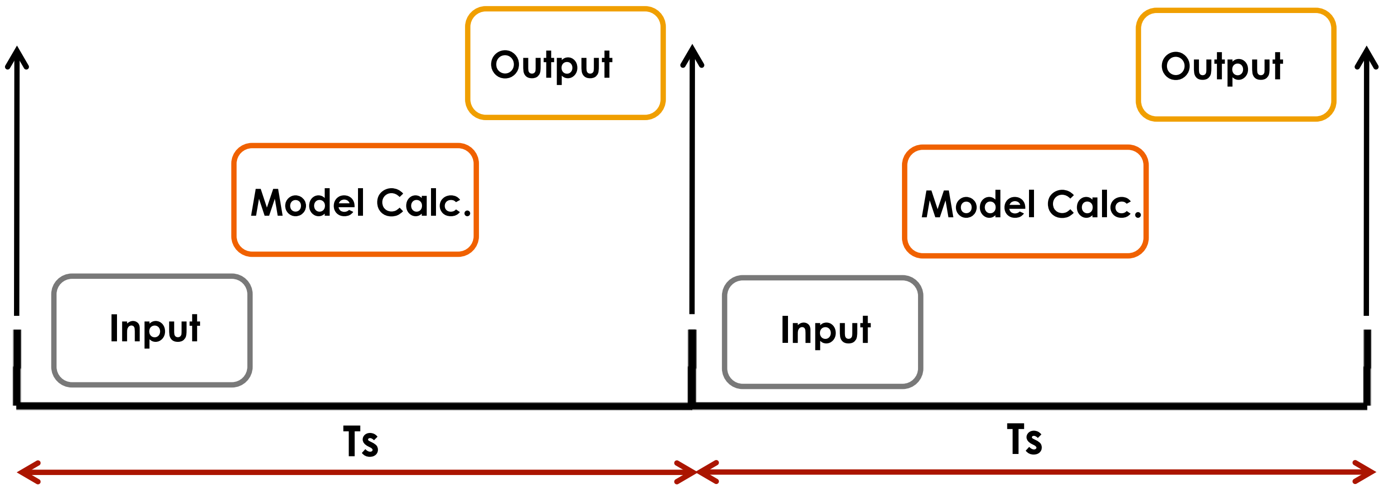
HIL simulation is a way of simulating systems where a part of the system is modeled and simulated in **real-time** while the remainder is the actual hardware connected in closed loop through various I/O interfaces (such as analog-to-digital – A/D – and digital-to-analog –D/A – converters, and signal conditioning equipment).



Hardware-in-the-Loop (HIL)

What is the Real-Time Simulation?

The Real-time simulation is a simulation task that all the involved "devices" (namely, reading inputs, model computations, and sending outputs) should be perform within each specific **simulation time-step** (**Ts**).



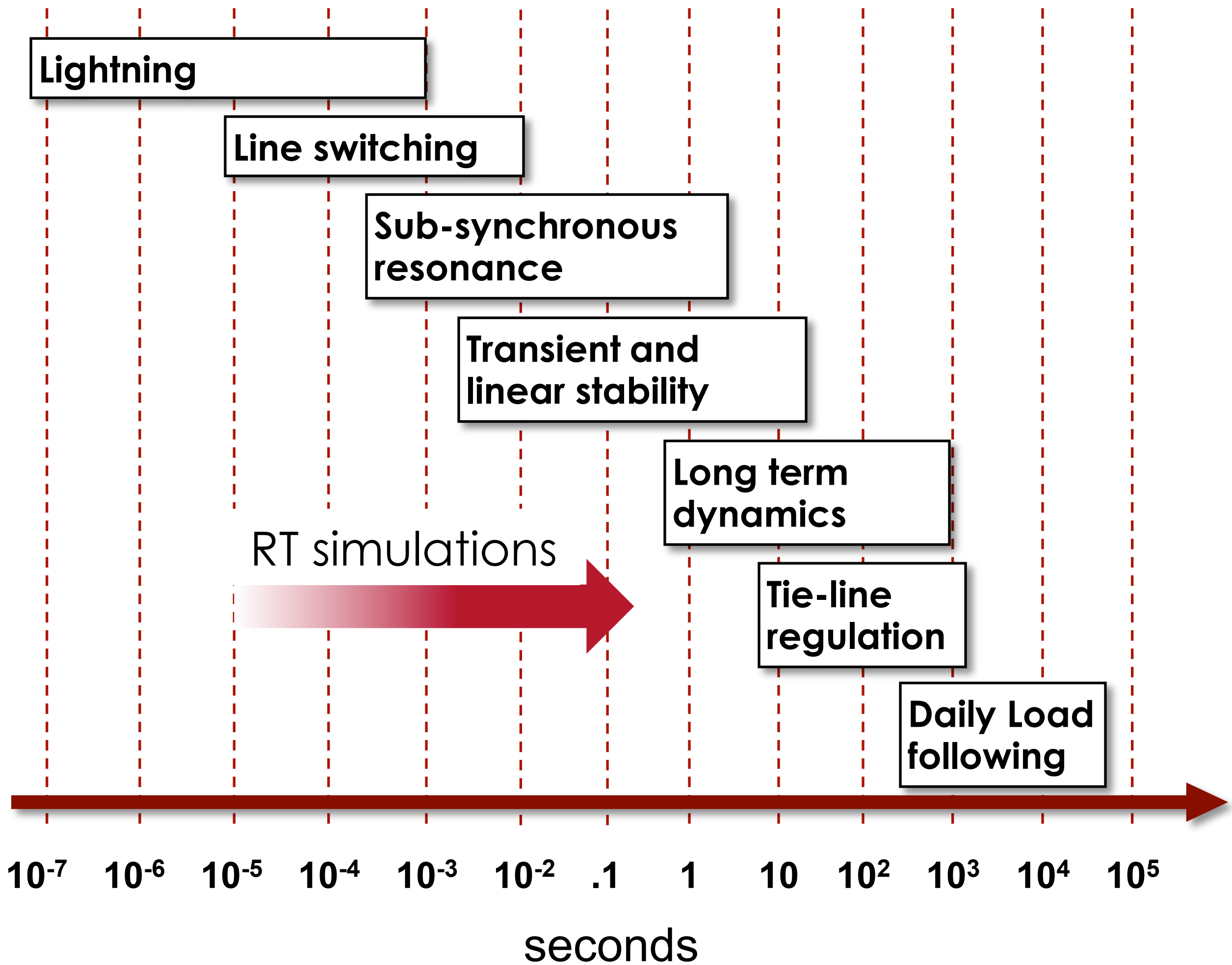
Hardware-in-the-Loop (HIL)

Advantages of HIL:

- ✓ Early testing of controllers when physical test benches are not available;
- ✓ Fast prototyping;
- ✓ Laboratory tests reduce time and cost and take place under controlled conditions;
- ✓ Avoid to subject the controller to risky contingencies;
- ✓ Tests are reproducible and can be automated.

Hardware-in-the-Loop (HIL)

What type of phenomena we can study ?



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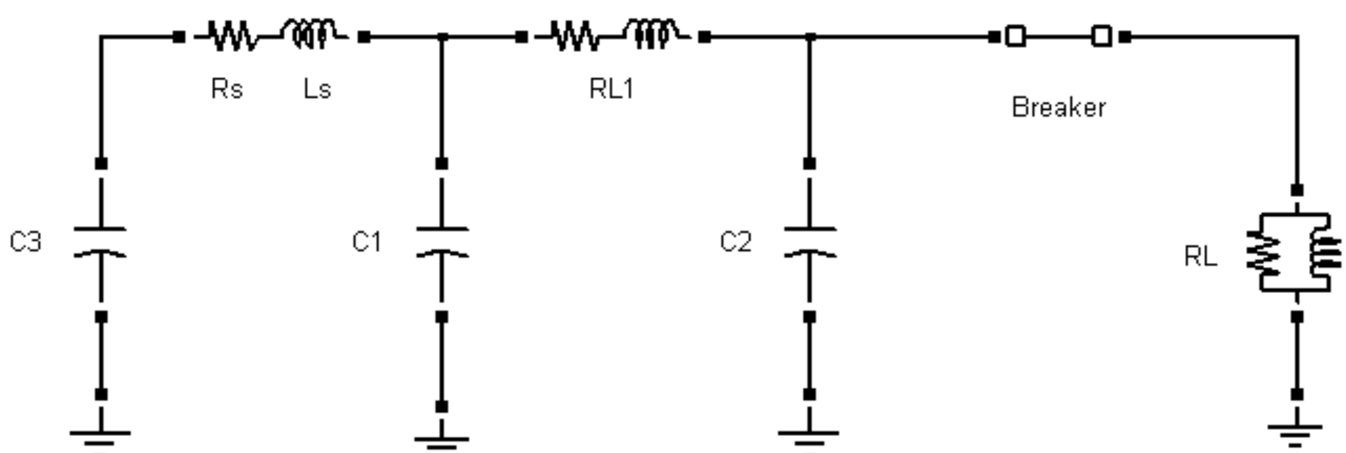
Numerical solvers

Generally, there are two approaches to represent and numerically solve electrical systems:

- Modified Nodal Analysis (MNA)
- State-Space Method



Numerical solvers

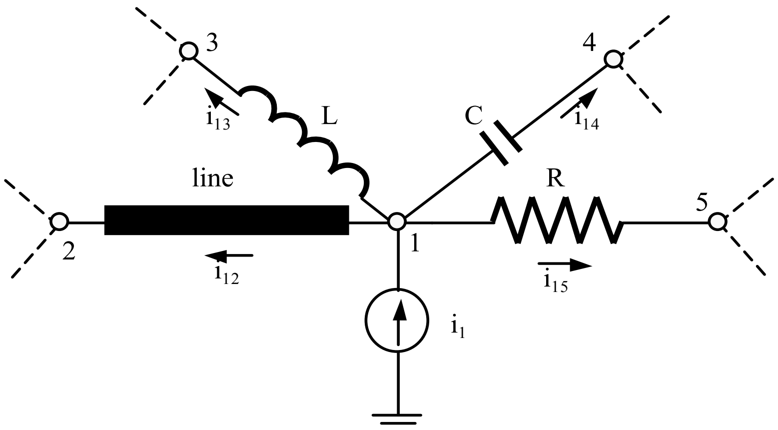
- **Modified Nodal Analysis (MNA):** each RLC branch is discretized based on the solver type (backward-forward Euler, trapezoidal, etc.)

Inductance equation within the interval $[t, t - \Delta t]$

$$i_{13}(t) = \frac{1}{L}\int_{-\infty}^{t}\left[v_1(t) - v_3(t)\right]dt =$$

$$= \frac{1}{L}\left(\int_{-\infty}^{t-\Delta t}\left[v_1(t) - v_3(t)\right]dt + \int_{t-\Delta t}^{t}\left[v_1(t) - v_3(t)\right]dt\right) =$$

$$= i_{13}(t-\Delta t) + \frac{1}{L}\int_{t-\Delta t}^{t}\left[v_1(t) - v_3(t)\right]dt$$



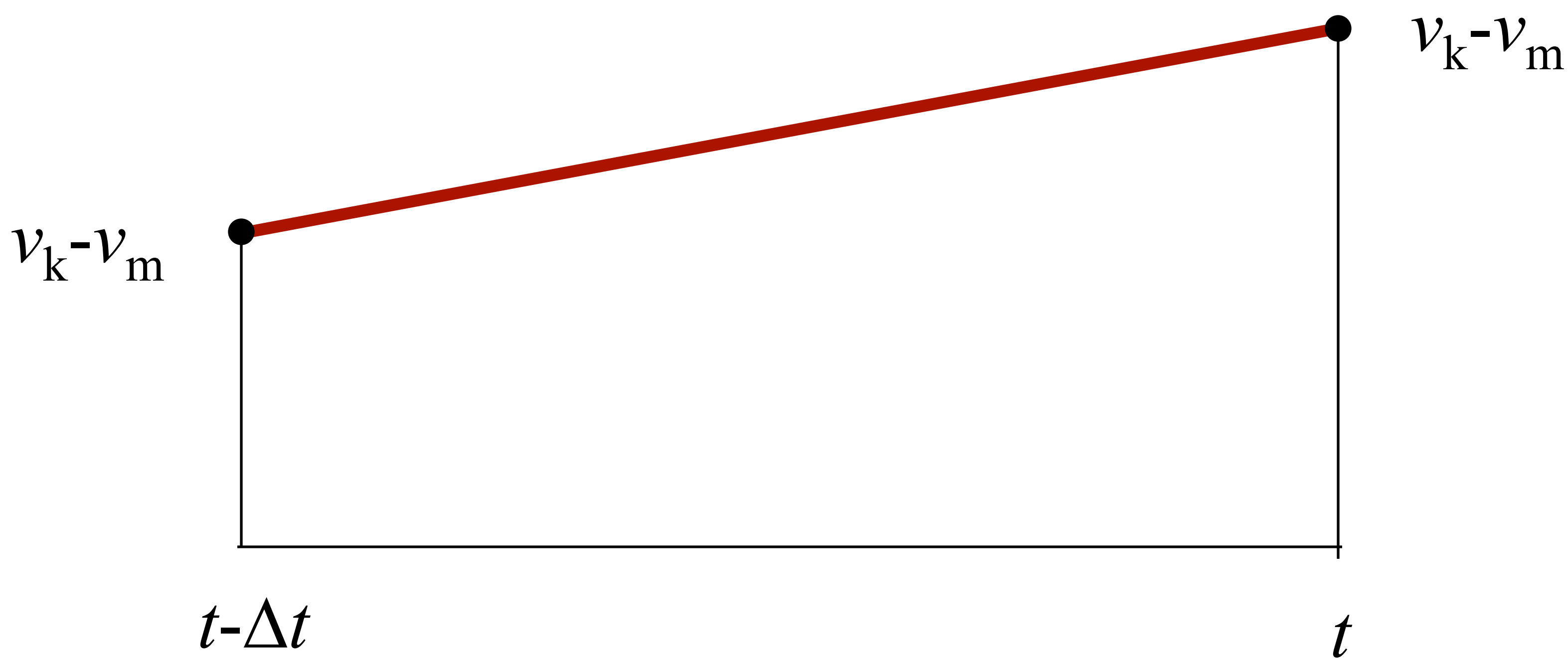
Capacitance equation within the interval $[t, t - \Delta t]$

$$v_1(t) - v_4(t) = \frac{1}{C}\int_{-\infty}^{t} i_{14}(t)dt = \frac{1}{C}\left(\int_{-\infty}^{t-\Delta t} i_{14}(t)dt + \int_{t-\Delta t}^{t} i_{14}(t)dt\right) =$$

$$= \left[v_1(t-\Delta t) - v_4(t-\Delta t)\right] + \frac{1}{C}\int_{t-\Delta t}^{t} i_{14}(t)dt$$

Numerical solvers

- **Modified Nodal Analysis (MNA):** example of numerical integration with the trapezoidal rule



$$\int_{t-\Delta t}^{t} \left[v_k(t) - v_m(t)\right] dt = \frac{\Delta t}{2}\left\{\left[v_k(t) - v_m(t)\right] + \left[v_k(t-\Delta t) - v_m(t-\Delta t)\right]\right\}$$

Numerical solvers

- **Modified Nodal Analysis (MNA):** example of numerical integration with the trapezoidal rule

Inductance

$$i_{13}(t) = I_{13}(t-\Delta t) + \frac{1}{L}\frac{\Delta t}{2}\left[v_1(t) - v_3(t)\right]$$

where

$$I_{13}(t-\Delta t) = i_{13}(t-\Delta t) + \frac{1}{L}\frac{\Delta t}{2}\left[v_1(t-\Delta t) - v_3(t-\Delta t)\right]$$

Capacitance

$$i_{14}(t) = \frac{2C}{\Delta t}\left[v_1(t) - v_4(t)\right] + I_{14}(t-\Delta t)$$

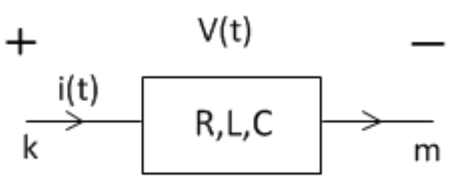
where

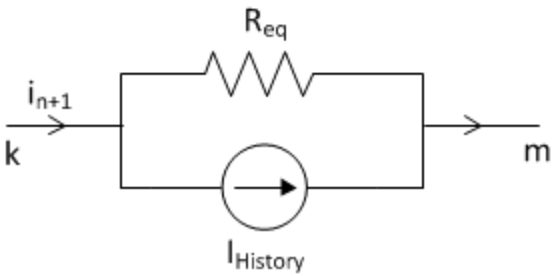
$$I_{14}(t-\Delta t) = i_{14}(t-\Delta t) - \frac{2C}{\Delta t}\left[v_1(t-\Delta t) - v_4(t-\Delta t)\right]$$

Numerical solvers

➢ **Modified Nodal Analysis (MNA)**

→ Each RLC branch is represented by an equivalent resistance in parallel with a specific current source. The value of the equivalent resistance and of the history terms depends to the integration method. In the table below we have reported the terms for the trapezoidal integration





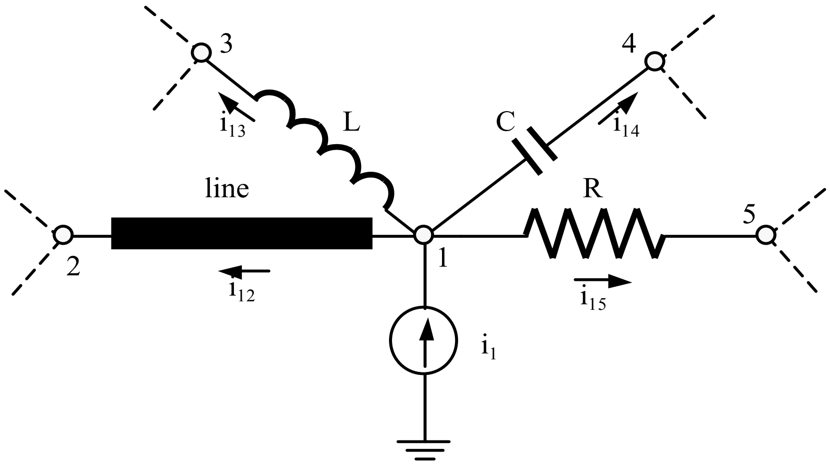
Element	R_{eq}	$I_{History}$
Resistor	R	-
Inductor	$\frac{2L}{\Delta t}$	$i_{13}(t-\Delta t)+\frac{1}{L}\frac{\Delta t}{2}\left[v_1(t-\Delta t)-v_3(t-\Delta t)\right]$
Capacitor	$\frac{\Delta t}{2C}$	$i_{14}(t-\Delta t)-\frac{2C}{\Delta t}\left[v_1(t-\Delta t)-v_4(t-\Delta t)\right]$

Numerical solvers

➢ **Modified Nodal Analysis (MNA)**

By explicating the current balance:

$$i_1(t) = i_{12}(t) + i_{13}(t) + i_{14}(t) + i_{15}(t)$$



Using the obtained algebraic equations for all the branch elements:

$$i_{12}(t) = \frac{1}{Z} v_1(t) + I_{12}(t-\tau)$$

$$i_{13}(t) = \frac{\Delta t}{2L}\left[v_1(t) - v_3(t)\right] + I_{13}(t-\Delta t)$$

$$i_{14}(t) = \frac{2C}{\Delta t}\left[v_1(t) - v_4(t)\right] + I_{14}(t-\Delta t)$$

$$i_{15}(t) = \frac{1}{R}\left[v_1(t) - v_5(t)\right]$$

Numerical solvers

➢ Modified Nodal Analysis (MNA)

- All branches are replaced by corresponding equivalent resistances
- For all nodes, a global matrix of admittance is built: $[\mathbf{Y}][v(t)]=[i(t)]-[\mathbf{I}]$
- Nodal voltages are found by solving this matrix problem, either by direct inversion or LU decomposition.
- Re-factorization of **Y** is required in case of a switch operations (→topology variation)

$$\begin{bmatrix} \frac{1}{R}+\frac{\Delta t}{2L}+\frac{2C}{\Delta t}+\frac{1}{Z} & 0 & -\frac{\Delta t}{2L} & -\frac{2C}{\Delta t} & -\frac{1}{R} \\ -\frac{1}{Z} & 0 & 0 & 0 & 0 \\ -\frac{\Delta t}{2L} & 0 & \frac{\Delta t}{2L} & 0 & 0 \\ -\frac{2C}{\Delta t} & 0 & 0 & \frac{2C}{\Delta t} & 0 \\ -\frac{1}{R} & 0 & 0 & 0 & \frac{1}{R} \end{bmatrix} \begin{bmatrix} v_1(t) \\ v_2(t) \\ v_3(t) \\ v_4(t) \\ v_5(t) \end{bmatrix} = \begin{bmatrix} i_1(t) \\ i_2(t) \\ i_3(t) \\ i_4(t) \\ i_5(t) \end{bmatrix} - \begin{bmatrix} I_{12}(t-\tau)+I_{13}(t-\Delta t)+I_{14}(t-\Delta t) \\ I_{12}(t-\tau) \\ I_{13}(t-\Delta t) \\ I_{14}(t-\Delta t) \\ 0 \end{bmatrix}$$

Numerical solvers

➢ **State-Space Method**

- Alternative representation of the differential equations that describe the system :

$$\dot{x} = A_k x + B_k u \qquad y = C_k x + D_k u$$

- k → matrix index associated to switch permutations;
- Numerical solution by means of different solvers:
  - *low order methods*, like the trapezoidal one, correspond in Simulink-SimPowerSystems to order 2;
  - *higher order methods* (order 5) are implemented in specific Simulink solvers (e.g. ARTEMiS) for RT applications (e.g. eMEGAsim).

Numerical solvers

- **State-Space Method**
  - Continuous-time state-space expression $\dot{x} = A_k x + B_k u$
    - Discretized solution for a generic integration time step Δt:

$$x_{n+1} = e^{\Delta t} x_n + \int_{t-\Delta t}^{t} e^{A(t-\tau)} B u(\tau) d\tau$$

- **Trapezoidal method (order 2):**

$$e^{A\Delta t} = \frac{I + A\Delta t / 2}{I - A\Delta t / 2}$$

- **ARTEMiS art5 method (order 5):**

$$e^{A\Delta t} = \frac{I + \frac{2}{5} A\Delta t + \frac{1}{20}(A\Delta t)^2}{I - \frac{3}{5} A\Delta t + \frac{3}{20}(A\Delta t)^2 - \frac{1}{60}(A\Delta t)^3}$$

Numerical solvers

- **MNA**
  - ✓ Easy to implement
  - ✓ Reduced computation time to prepare the $[\mathbf{Y}]$ matrix
  - ✓ Dynamic re-factorization of the $[\mathbf{Y}]$ Matrix to consider the switches

- **State-Space**
  - ✓ More difficult to implement
  - ✓ Larger computational time to generate the state equations
  - ✓ Can be implemented with different solvers and in variable-step
  - ✓ More stable and accurate than the MNA

Numerical solvers

- **Solvers used in commercial simulators**
  - ✓ Classical nodal technique (RTDS)
  - ✓ State-Space with order 5 (eMEGAsim)
  - ✓ Two-Level State-Space Nodal with Norton Equivalent (eMEGAsim)
- **Solvers used in R&D Center and universities**
  - ✓ Classical nodal technique (Hypersim)
  - ✓ MATE: two level nodal technique with Thevenin equivalent (Marti)
  - ✓ GENE: Two-level nodal technique with Norton equivalent

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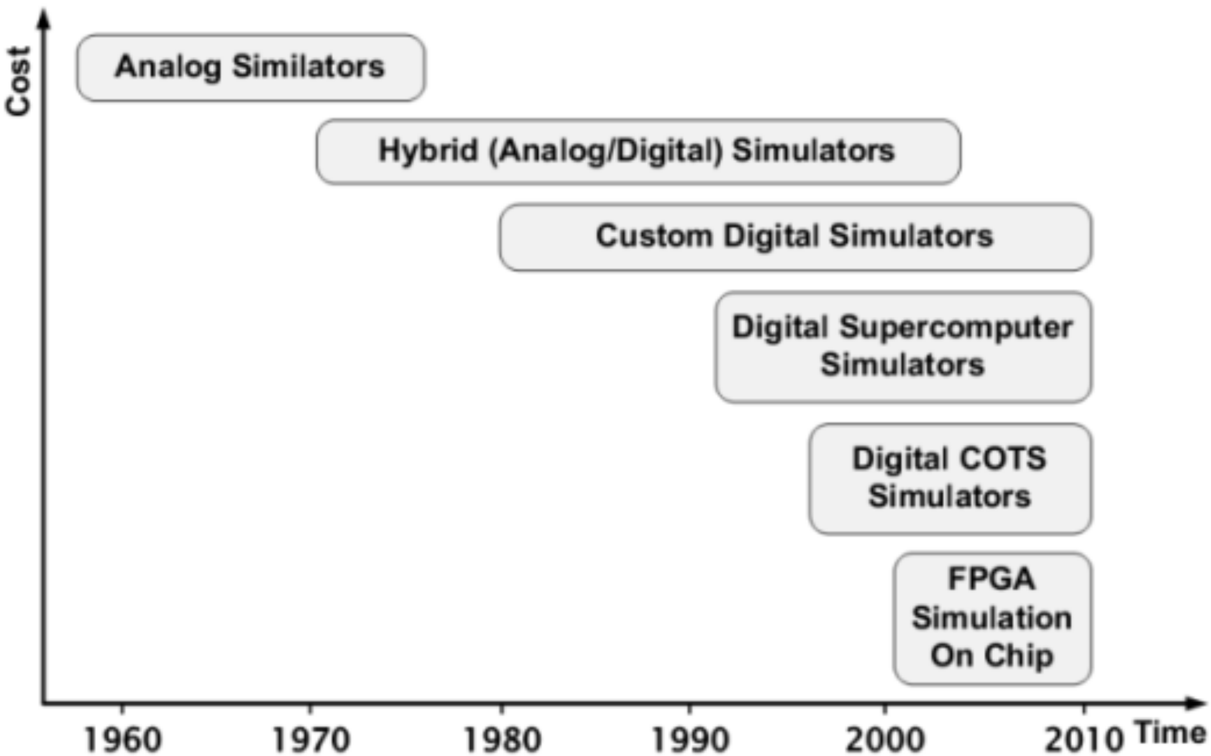
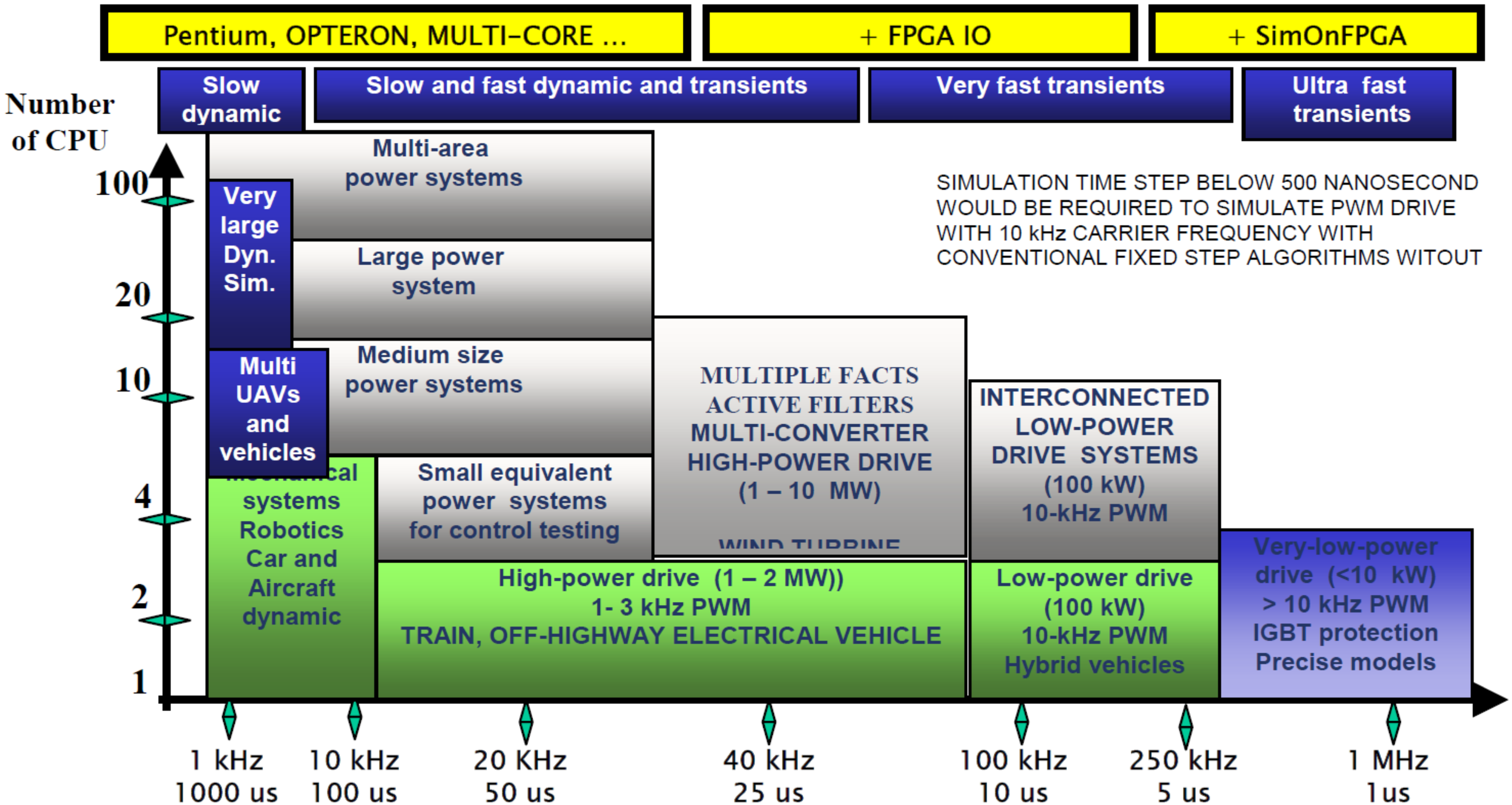
Evolution of Real-Time Digital Simulators



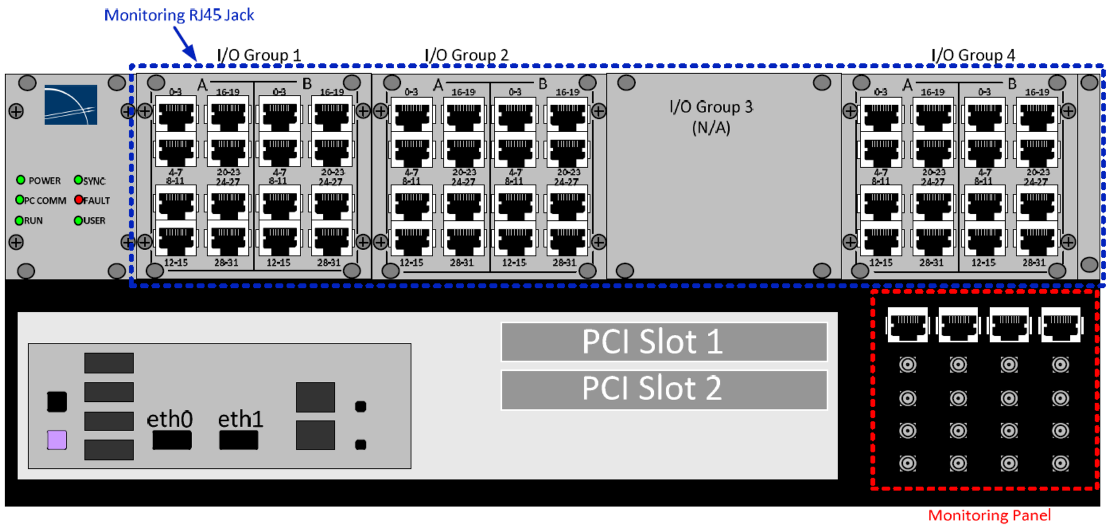
Hardware

Evolution of Real-Time Digital Simulators



Hardware

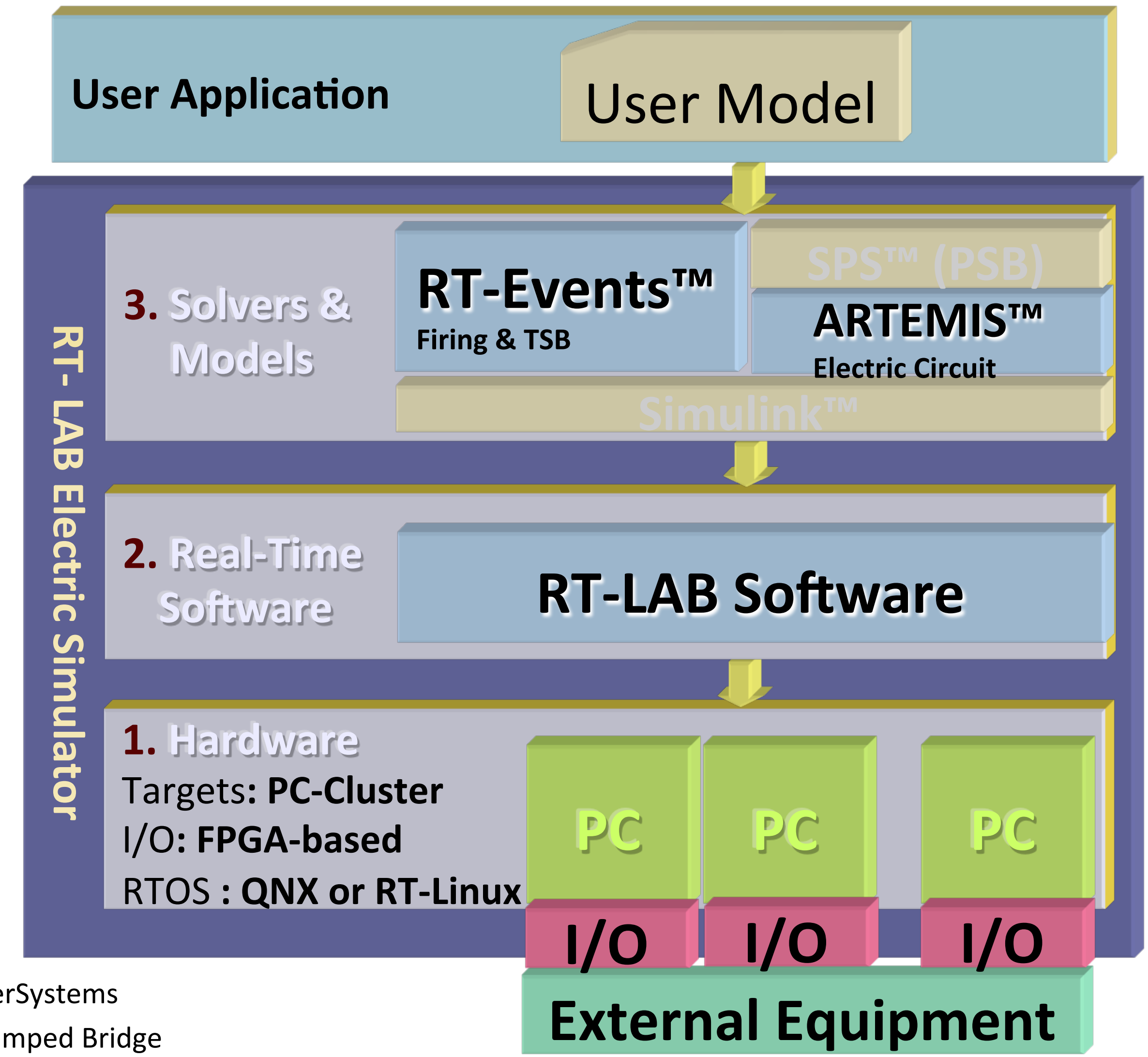
Opal-RT eMEGAsim



Items	Quantity	Description
Operating System		Redhat V 2.6.29.6-Opalrt-5
Chassis Type		OP5600 chassis
CPU	2	Intel Xeon 6-core 3.46GHz 12M cache
Total Core #	12	
Memory	4	1 GB
Motherboard		X8DAL-I-O Supermicro Motherboard Dual Xeon

Hardware

eMEGAsim



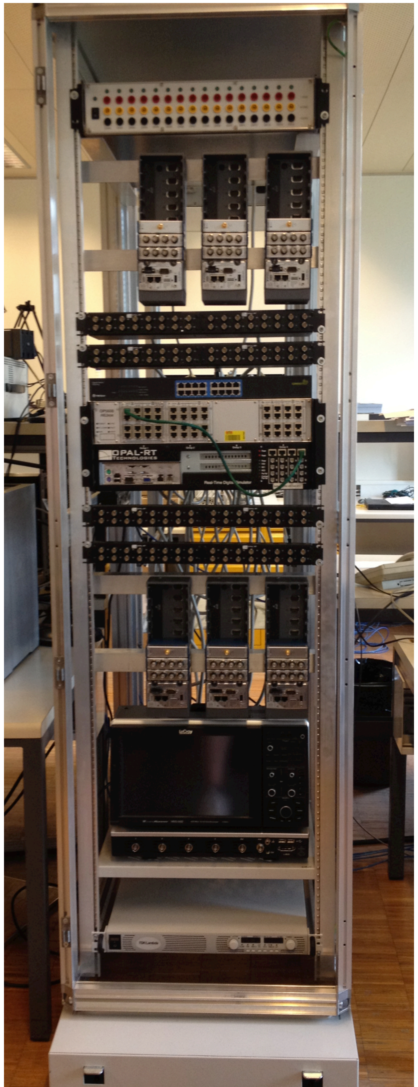
SPS: SimPowerSystems

TSB: Time-Stamped Bridge

Hardware

Opal-RT eMEGAsim at the EPFL-DESL

Opal-RT eMEGAsim
power grid real-time digital simulator
Specs.
Max nr. of 200 nodes
Max nr. Switches: 150 switches
Typical Rt integration time times 10 – 50 μs



Aims

- *monitoring*: based on the use of phasor measurement units (PMUs);
- *network observation*: RT-state estimation;
- *controls*: optimal voltage control, congestion management, optimal network configuration/ topology;
- *protections*: PMU-based relaying schemes, fault location.

Hardware

Limitations of the CPU-based systems

- ✓ **Minimum simulation time step > 10 µs**
- ✓ **Reduced frequency bandwidth**

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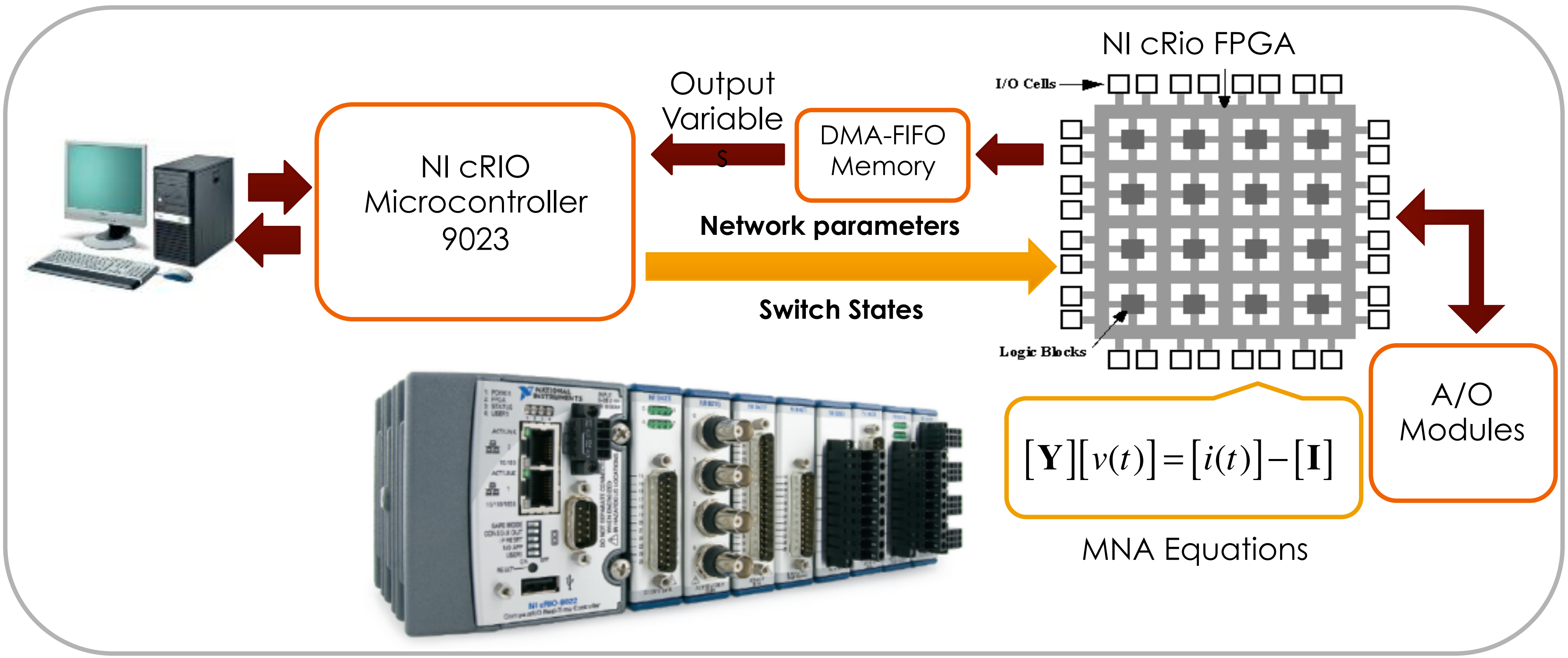
FPGA-Based RDTS

Hardware

FPGA-Based RTDS



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Real-time simulators are able to reproduce in real-time the behaviour of complex electrical power networks with reference to the following conditions:

- steady-state;
- electromechanical transients;
- electromagnetic transients.

These systems represents the state-of-the-art to study the RT response of modern and future power systems and will play a fundamental role in the development of the future electrical infrastructure.